What is claimed is:

1. A semiconductor device manufacturing method comprising the steps of:

forming a first dielectric film on an entire upper part of a semiconductor substrate; forming a photoresist pattern on a p-well including a gate pattern of an NMOS transistor and a gate spacer thereof, and subsequently implanting ions into an n-well for forming a high concentration source/drain regions of a PMOS by using the first dielectric film formed on upper parts of a gate pattern and a gate spacer of a PMOS transistor as an implant mask; and

forming an interlayer dielectric film thereon and then forming a contact,

wherein said semiconductor substrate includes a PMOS transistor region in the n-well; an NMOS transistor region in the p-well; the gate pattern of the PMOS transistor formed on the PMOS transistor region and the gate spacers formed on both side walls of the gate pattern thereof, and the gate pattern of the NMOS transistor formed on the NMOS transistor region and the gate spacers formed on both side walls of the gate pattern thereof; the n-well having a low concentration source/drain regions formed by ion-implantation using the gate pattern of the PMOS transistor as an implant mask; and the p-well having a low concentration source/drain regions formed by ion-implantation using the gate pattern of the NMOS transistor as an implant mask and a high concentration source/drain regions formed by ion-implantation using the gate pattern and the gate spacers of the NMOS

transistor as an implant mask.

2. The method as claimed in claim 1, wherein the first dielectric film is an etch stopper in forming a contact hole as well as the implant mask in forming the high concentration source/drain regions of the PMOS transistor.

3. The method as claimed in claim 1, wherein the first dielectric film thickness is 1000 Angstroms.

4. The method as claimed in claim 1, wherein the first dielectric film is made of any one of SiN and SiON.

5. A semiconductor device manufacturing method comprising the step of:

forming a high concentration source/drain regions of a PMOS transistor by an ion-implantation using a dielectric film formed on an entire upper part of a semiconductor substrate as an implant mask,

wherein the semiconductor substrate includes a PMOS transistor region in which a low concentration source/drain regions are ion-implanted into an n-well by using a gate pattern as an implant mask; and an NMOS transistor region, in which a low concentration source/drain regions are formed by an ion-implantation using a gate pattern of the NMOS transistor as an implant mask and a high concentration source/drain regions formed by ion-implantation using the gate pattern and gate spacers of the NMOS transistor as an implant mask.

6. A semiconductor device manufacturing method comprising the steps of:

forming a metal film on upper parts of a gate pattern of a PMOS transistor and a gate pattern of an NMOS transistor on a semiconductor substrate, and then forming a capping layer entirely over the semiconductor substrate including the gate patterns and gate spacers of the NMOS and PMOS transistors for performing a silicidation process and forming a silicide film on the upper parts of the gate patterns of the PMOS and NMOS transistors;

forming a photoresist pattern on a p-well including the gate pattern of the NMOS transistor and a gate spacer, and subsequently implanting ions into an n-well for forming a high concentration source/drain regions by using as an implant mask the capping layer formed on the upper parts of the gate pattern and a gate spacer of the PMOS transistor; and

forming an interlayer dielectric film thereon and then forming a contact,

wherein said semiconductor substrate includes a PMOS transistor region in the n-well; an NMOS transistor region in the p-well; the gate pattern of the PMOS transistor formed on the PMOS transistor region and the gate spacers formed on both side walls of the gate pattern thereof, and the gate pattern of the NMOS transistor formed on the NMOS transistor region and the gate spacers formed on both side walls of the gate pattern thereof; the n-well having a low concentration source/drain regions formed by ion-

implantation using the gate pattern of the PMOS transistor as an implant mask; and the p-well having a low concentration source/drain regions formed by ion-implantation using the gate pattern of the NMOS transistor as an implant mask and a high concentration source/drain regions formed by ion-implantation using the gate pattern and the gate spacers of the NMOS transistor as an implant mask.

7. The method as claimed in claim 6, wherein the capping layer is made of any one of SiN and SiON.

8. The method as claimed in claim 6, wherein the metal film is made of cobalt.

9. The method as claimed in claim 6, wherein the capping layer thickness is 1000 Angstroms.

10. The method as claimed in claim 6, wherein the capping layer is an etch stopper in forming a contact hole.

11. A semiconductor device comprising:

a semiconductor substrate having a uniform conductivity;

a PMOS transistor that includes a gate pattern composed of a gate oxide film and a gate conductive layer on a PMOS transistor region of the semiconductor substrate, ion-implanted low concentration source/drain regions formed on both sides of the gate pattern on the semiconductor

substrate, and ion-implanted high concentration source/drain regions also formed on both sides of the gate pattern but at a distance far from the gate pattern; and

an NMOS transistor that includes a gate pattern composed of a gate oxide film and a gate conductive layer on an NMOS transistor region of the semiconductor substrate, ion-implanted low concentration source/drain regions formed on both sides of the gate pattern on the semiconductor substrate, and ion-implanted high concentration source/drain regions also formed on both sides of the gate pattern but at a distance relatively nearer to the gate pattern compared to the distance between the high concentration source/drain regions and the gate pattern of the PMOS transistor.

12. A semiconductor device comprising:

a semiconductor substrate having a uniform conductivity; and

a PMOS transistor that includes a gate pattern composed of a gate oxide film and a gate conductive layer on a PMOS transistor region of the semiconductor substrate, a gate spacer on both sidewalls of the gate pattern, ion-implanted low concentration source/drain regions formed on both sides of the gate pattern in the semiconductor substrate, and ion-implanted high concentration source/drain regions also formed on both sides of the gate pattern but away from the gate spacer.

13. A semiconductor device manufacturing method comprising the steps of:

forming a first dielectric film on an entire upper part of a

semiconductor substrate that includes a PMOS transistor region, a gate pattern of a PMOS transistor formed on the PMOS transistor region, an n-well having ion-implanted low concentration source/drain regions formed by using the gate pattern of the PMOS transistor as an implant mask, and spacers formed on both side walls of the gate pattern;

implanting ions for forming a high concentration source/drain regions into the n-well by using as an implant mask the first dielectric film formed on upper parts of the gate pattern of the PMOS transistor and the gate spacers; and

forming an interlayer dielectric film thereon, and subsequently forming a contact.

14. A semiconductor device characterized by a low concentration source/drain regions formed by using a gate pattern as an implant mask, a dielectric film formed on an entire upper part of a semiconductor substrate on which gate spacers are formed on both side walls of the gate pattern, and high concentration source/drain regions formed by using the dielectric film as an implant mask.